Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A circuit board device having a power supply region divided into two or more power supply regions by a slit and a ground region adjacent to the power supply region, wherein, when at least one region of said two or more power supply regions and the ground region that are adjacent has a shape that may be considered a track having a length that is larger than its width, a terminal element having an impedance that is substantially equal to a characteristic impedance between said at least one region and said ground region is connected between said power supply region and said ground region at a terminal end of said at least one region.

2. (Withdrawn) The circuit board device according to claim 1, further comprising a dielectric layer, wherein the power supply region and the ground region that are adjacent are formed in different layers with the dielectric layer interposed therebetween and substantially oppose one another and overlap.

3. (Withdrawn) The circuit board device according to claim 1, further comprising a circuit, which has a plurality of via holes that forms a parallel circuit, formed adjacent to the terminal portion, and the terminal element is connected between the layer via the parallel circuit.

4. (Canceled)

5. (Original) The circuit board device according to claim 1, wherein the terminal element includes a capacitor.

6. (Original) The circuit board device according to claim 1, wherein the terminal element includes a resistor and a capacitor which are series-connected.

7. (Canceled)

8. (Currently Amended) The circuit board device according to claim 1, wherein an impedance Zr of the terminal element is set such ~~that a~~ that the characteristic impedance Ze and the impedance Zr of the terminal element satisfy a relationship $0.1 \leq Zr/Ze \leq 10$.

9. (Currently Amended) The circuit board device according to claim 6, wherein a relationship ~~between a~~ between the characteristic impedance Ze and a resistance R of the resistor satisfies $(Ze/5) \leq R \leq (5 \cdot Ze)$, and a capacity C of the capacitor satisfies $C \geq 1/(10\pi \cdot f_{min} \cdot Ze)$, where f_{min} is a lower limit of a radiation noise frequency of a reduction target.

10-14. (Canceled).

15. (Currently Amended) A circuit board device having a power supply region and a ground region that are adjacent and are formed in the same plane, wherein, when at least one region of the power supply region and the ground region that are adjacent has a shape that may be considered a track, a terminal element having an impedance that is substantially equal to a characteristic impedance between said regions is connected between the power supply region and the ground region at a terminal ~~portion vicinity~~ end of said at least one region.

16. (Previously Presented) The circuit board device according to claim 15, wherein the terminal element includes a capacitor.

17. (Previously Presented) The circuit board device according to claim 15, wherein the terminal element includes a resistor and a capacitor which are series-connected.

18. (Previously Presented) The circuit board device according to claim 15, wherein the region that may be considered a track is a shape having a length that is larger than a width.

19. (Currently Amended) The circuit board device according to claim 15, wherein ~~an~~ the impedance Zr of the terminal element is set such ~~that a~~ that the characteristic

impedance Ze and the impedance Zr of the terminal element satisfy a relationship $0.1 \leq Zr/Ze \leq 10$.

20. (Currently Amended) The circuit board device according to claim 17, wherein a relationship ~~between a~~ between the characteristic impedance Ze and a resistance R of the resistor satisfies $(Ze/5) \leq R \leq (5 \cdot Ze)$, and a capacity C of the capacitor satisfies $C \geq 1/(10\pi \cdot f_{min} \cdot Ze)$, where f_{min} is a lower limit of a radiation noise frequency of a reduction target.

21. (Previously Presented) The circuit board device according to claim 1, wherein the slit has a T-shape.

22. (Previously Presented) The circuit board device according to claim 15, wherein the power supply region is entirely surrounded by the ground region.

23. (Previously Presented) The circuit board device according to claim 15, wherein the power supply region and the ground region face each other without overlapping.

24. (Previously Presented) The circuit board device according to claim 15, wherein the power supply region and the ground region have the same shape.

25. (Previously Presented) The circuit board device according to claim 1, wherein terminal element is connected between said power supply region and said ground region only at said terminal end of said at least one region.

26. (Previously Presented) The circuit board device according to claim 1, wherein an outer periphery of said power supply region and said ground region is free from connection by said terminal element.

27. (Previously Presented) The circuit board device according to claim 15, wherein the terminal element is connected between said power supply region and said ground region only at said terminal end of said at least one region.

28. (Previously Presented) The circuit board device according to claim 15, wherein an outer periphery of said power supply region and said ground region is free from connection by said terminal element.

Amendments to the Drawings:

The attached replacement drawing sheets makes changes to Figs. 6A. 6B, 12 and 13 and replaces the original sheets with Figs. 6A, 6B, 12 and 13.

Attachment: Replacement Sheets